WHAT ARE

FIELD PROGRAMMABLE

Audible plays called at the line of scrimmage?

Signaling for a squeeze bunt in the ninth inning?

They’re none of the above!

We’re going to take a look at:

Field Programmable GATE ARRAYS (FPGAs)

The FPGA

What is it, and why do we care?

The FPGA

- First of all, why do we care?
  - Some of the "cutting edge" developments in amateur radio equipment involve FPGAs.
  - Three Software Defined Radios (SDRs) are examples.
    - First the HPSDR Hermes transceiver, and the ANAN-10 and ANAN-100
    - Second ANGELIA and the ANAN-100D
    - Third the Flex-Radio Models 6500 and 6700

HPSDR

- HPSDR means High Performance Software Defined Radios
- It's a collection of "open source" hardware and software projects designed by interested experimenters worldwide.
- Hermes is one of the latest projects.
- The first Hermes boards were sold by TAPR, the Tuscon Amateur Packet Radio group in late 2012.
- Now supplied by Apache Labs in Haryana, India
- Models now available with 10W and 100W amplifiers called ANAN-10 and ANAN-100

ANAN-10 and ANAN-100

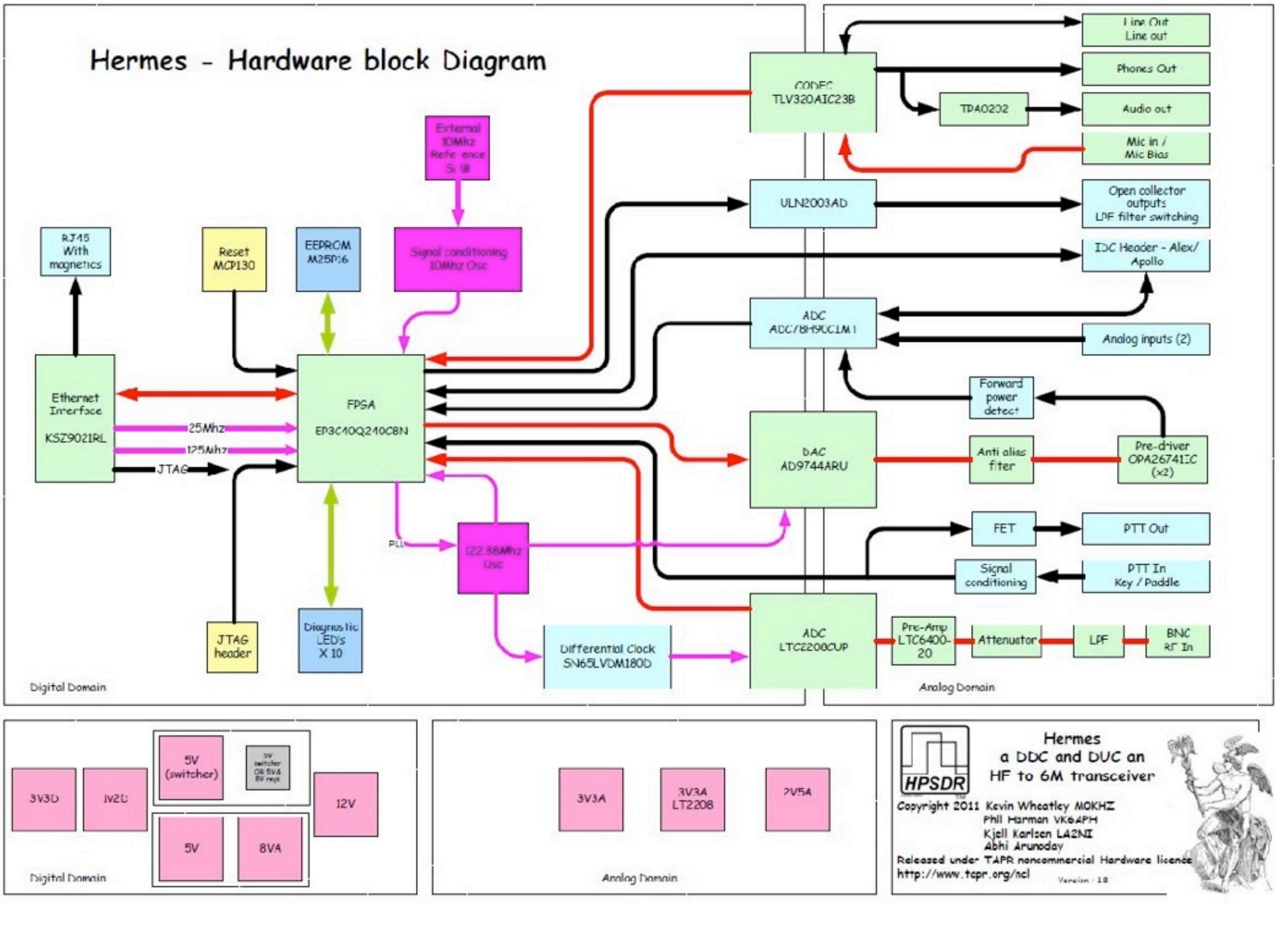
Hermes + 10 Watt Amplifier

Hermes + 100 Watt Amplifier

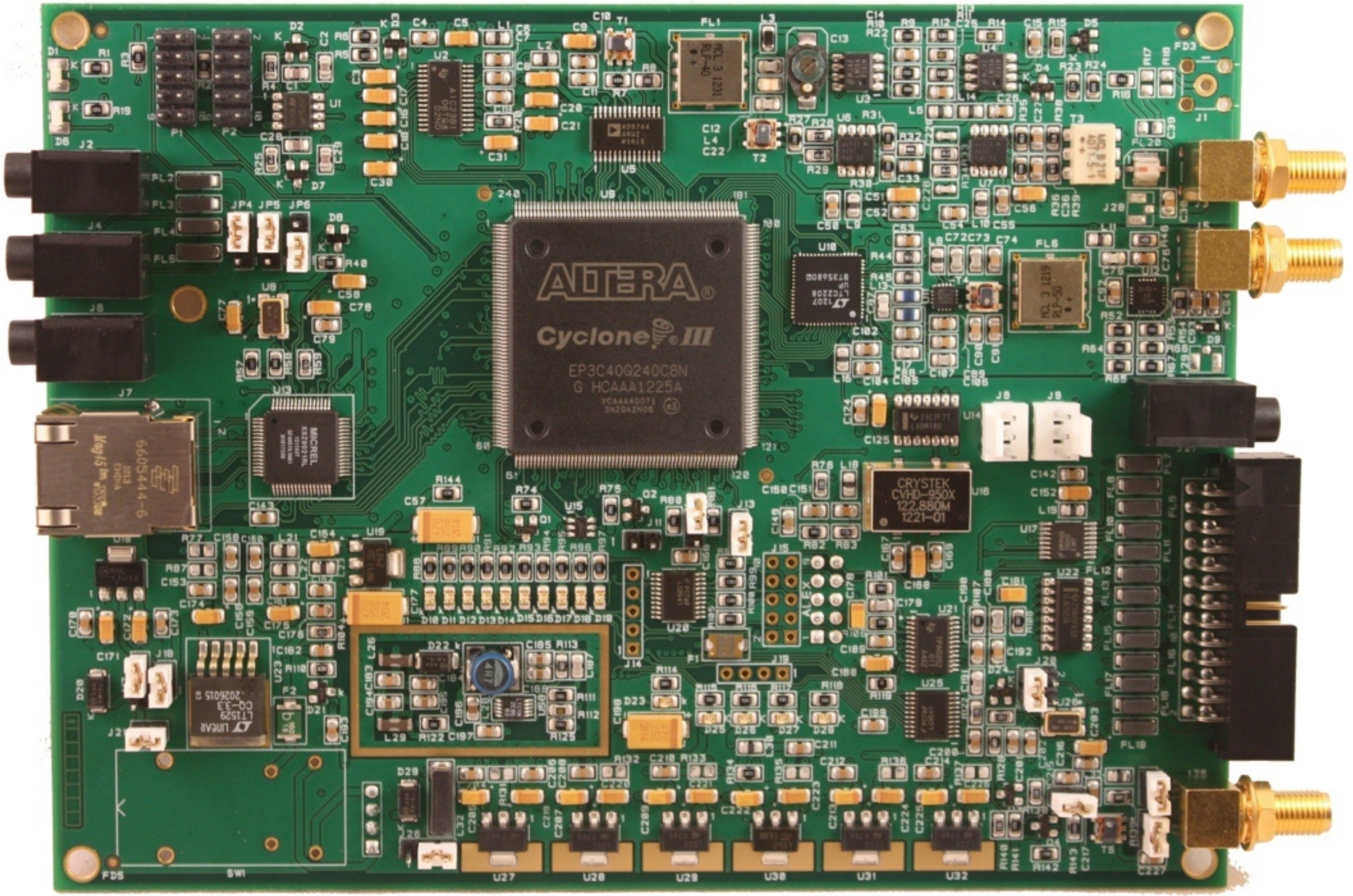
HERMES

- Not a traditional superheterodyne architecture
- (DDC) Direct-Down Conversion Receiver
- (DUC) Direct-up Conversion 500 mW transmitter
- Gigabit Ethernet Internet Interface
- On a single 8-layer 12 cm x 16 cm printed circuit board
- Coverage from 50kHz to 55MHz
- AM, FM, RTTY, CW, LSB, USB, Digital
- Supports multiple receivers
  - sharing one antenna
  - with suitable software
- Current user-software is free

HERMES


Hermes - Hardware block Diagram
External 10Mhz Reference Sig IP
RJ45 With magnetics
Reset MCP130
EEPROM M25P16
Signal conditioning 10Mhz Osc
Ethernet Interface KSZ9021RL
25Mhz
125Mhz
JTAG
FPGA EP3C40Q240C8N
PLL
122.88Mhz Osc
JTAG header
Diagnostic LED's X 10
Differential Clock SN65LVDM180D
CODEC TLV320AIC23B
ULN2003AD
ADC AD9744ARU
ADC LTC2208CUP
Line Out Line out
Phones Out
TPA0202
Audio out
Mic in / Mic Bias
Open collector outputs LPF filter switching
IDC Header - Alex/ Apollo
ADC AD6645
Analog inputs (2)
Forward power detect
Anti alias filter
Pre-driver OPA2674IC (x2)
FET
PTT Out
Signal conditioning
PTT In Key / Paddle
Pre-Amp LTC6400-20
Attenuator
LPF
BNC RF In
Digital Domain
Analog Domain
3V3D
1V2D
5V (switcher)
5V switcher OR 5V& 8V regs
12V
5V
8V4
Digital Domain
3V3A
3V3A LT2208
2V5A
Analog Domain
HPSDR
Hermes
a DDC and DUC an
HF to 6M transceiver
Copyright 2011 Kevin Wheatley M0KHZ
Phil Harman VK6APH
Kjell Karlsen LA2NI
Abhi Arunoday
Released under TAPR noncommercial Hardware licence
http://www.tapr.org/ncl
Version : 1.0

HERMES


ALTERA
Cyclone III
EP3C40Q240C8N
G HCAAA1225A
CRYSTEK
CVHD-950X
122.880M
1221-01

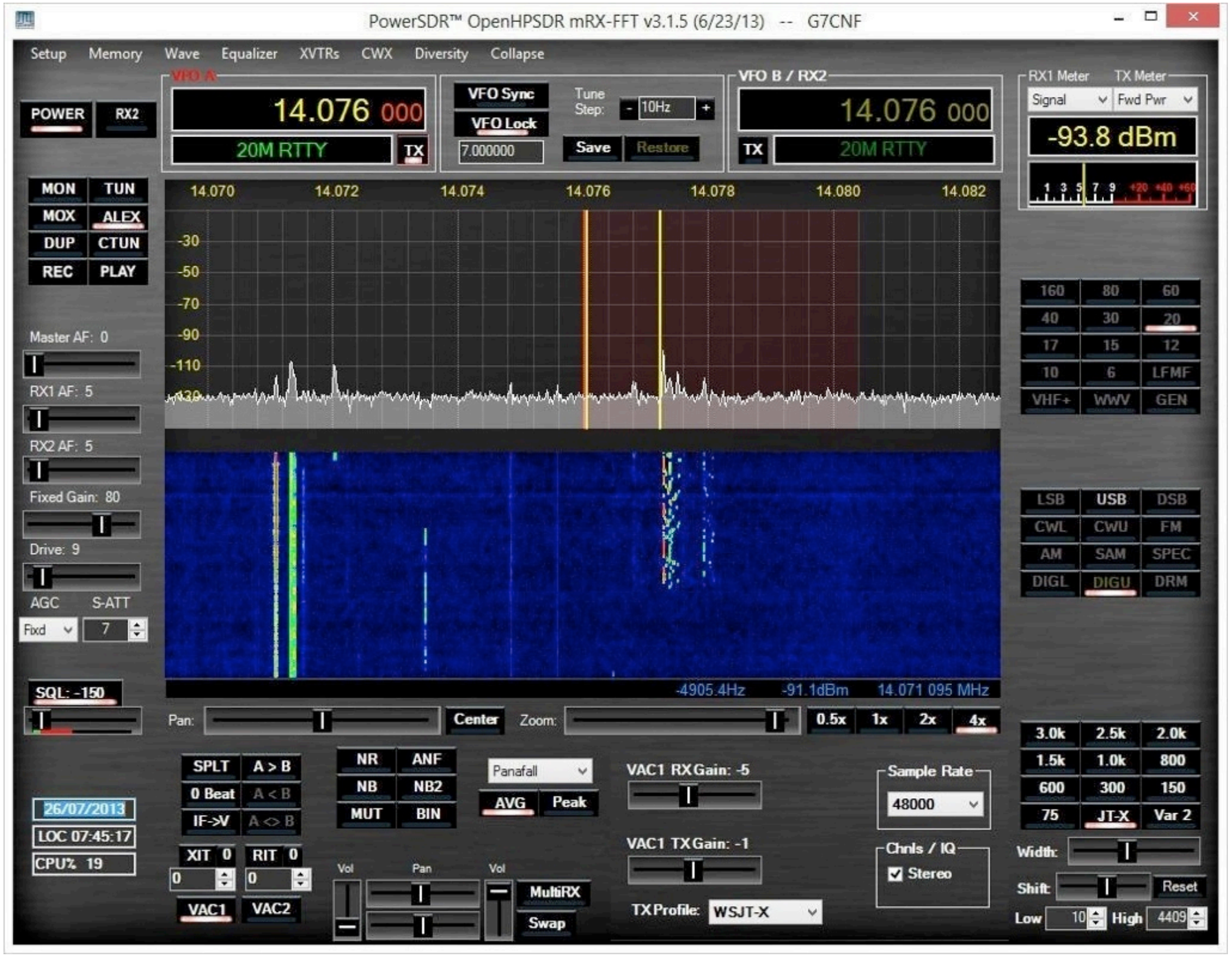
ALTERA EP3C40Q240C8N

- Number of Logic Blocks (CLBs)* - 2475
- Number of Logic Elements - 39,600
- Number of I/Os - 128
- Package - Plastic Quad Flat Pack with 240 pins
- Price - $78.50

* CLB means Configurable Logic Block...more about that later!

- Verilog code for Hermes written by Phil Harman, VK6APH, from Perth, Australia

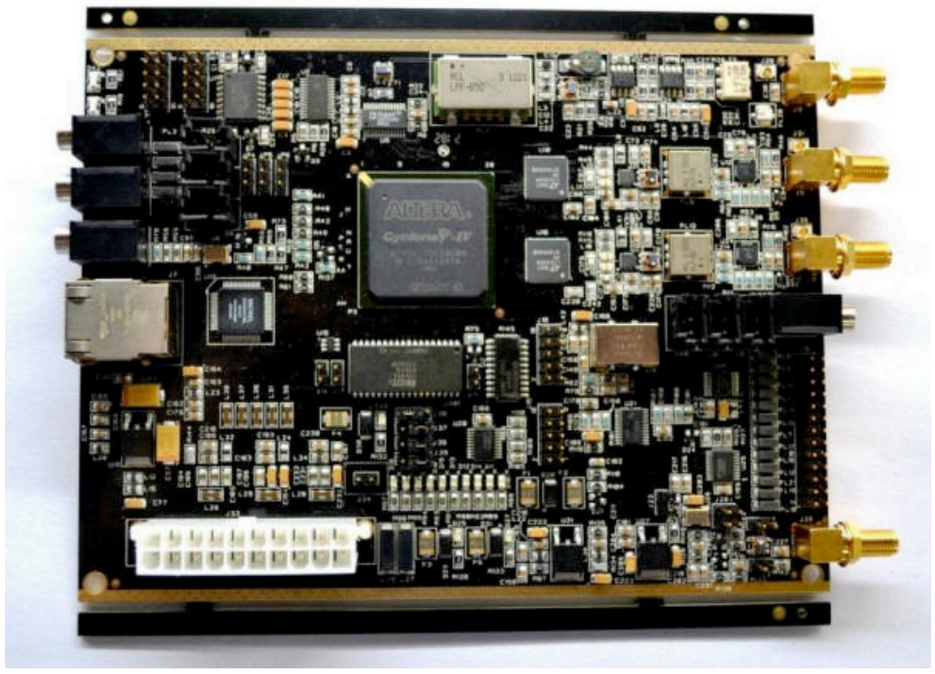
HERMES



- Flex Radio's PowerSDR software adapted primarily by Bill Tracey, KD5TFD and Doug Wigley, W5WC

ANGELIA

- 4th Generation DDC/DUC Transceiver Board
- In Apache Labs ANAN-100D 100 W Transceiver
- Has Dual Analog-to-Digital Converters
- Capable of 7 Simultaneous Receivers
- Allows Synchronizing Receivers for Coherent Receiver Operations (Diversity & Beam Steering)



Angelia

ANAN-100D

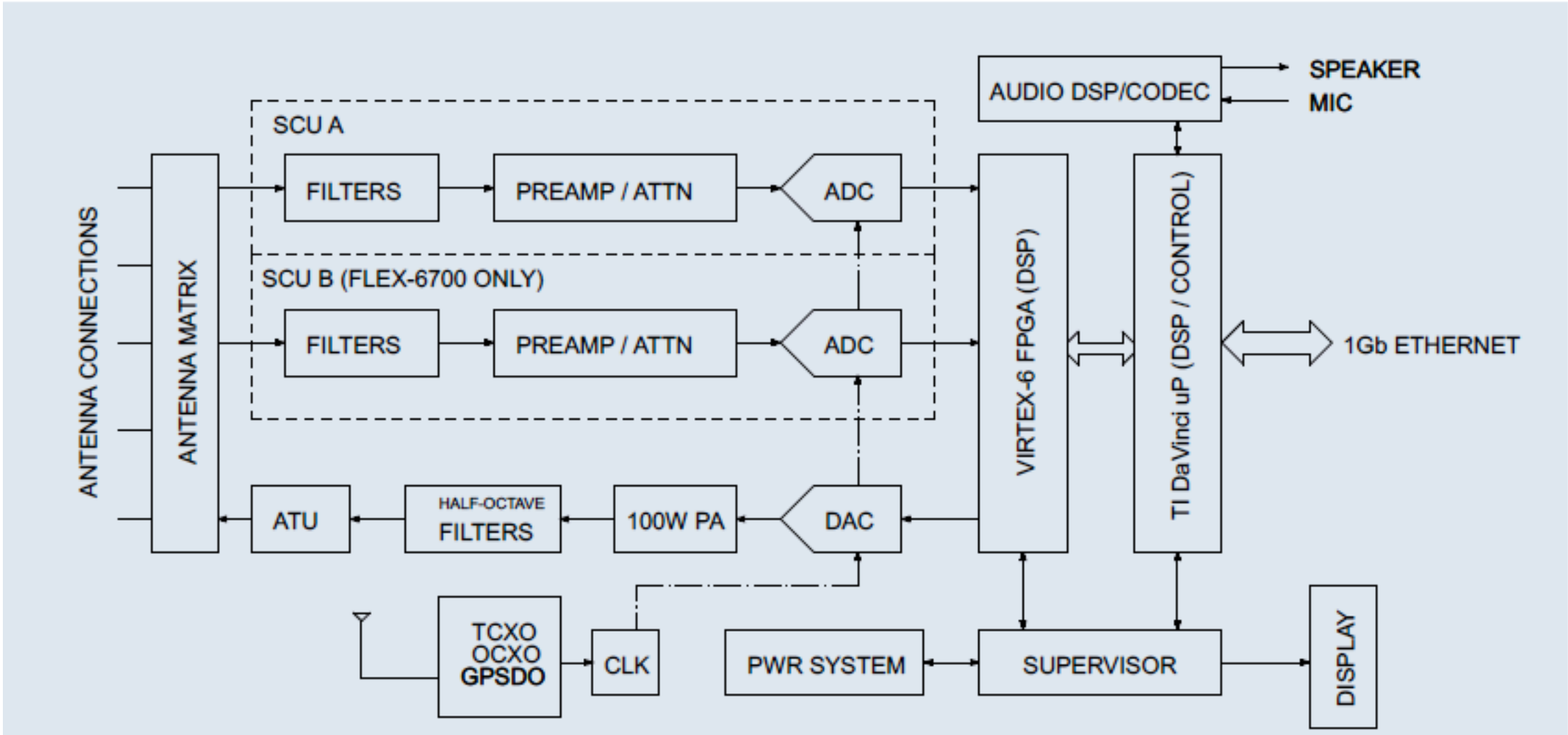
cuSDR Software with Angelia

- 7 “slice” receivers
- cuSDR beta software (RX only) written by Hermann, DL3HVH

FLEX 6000

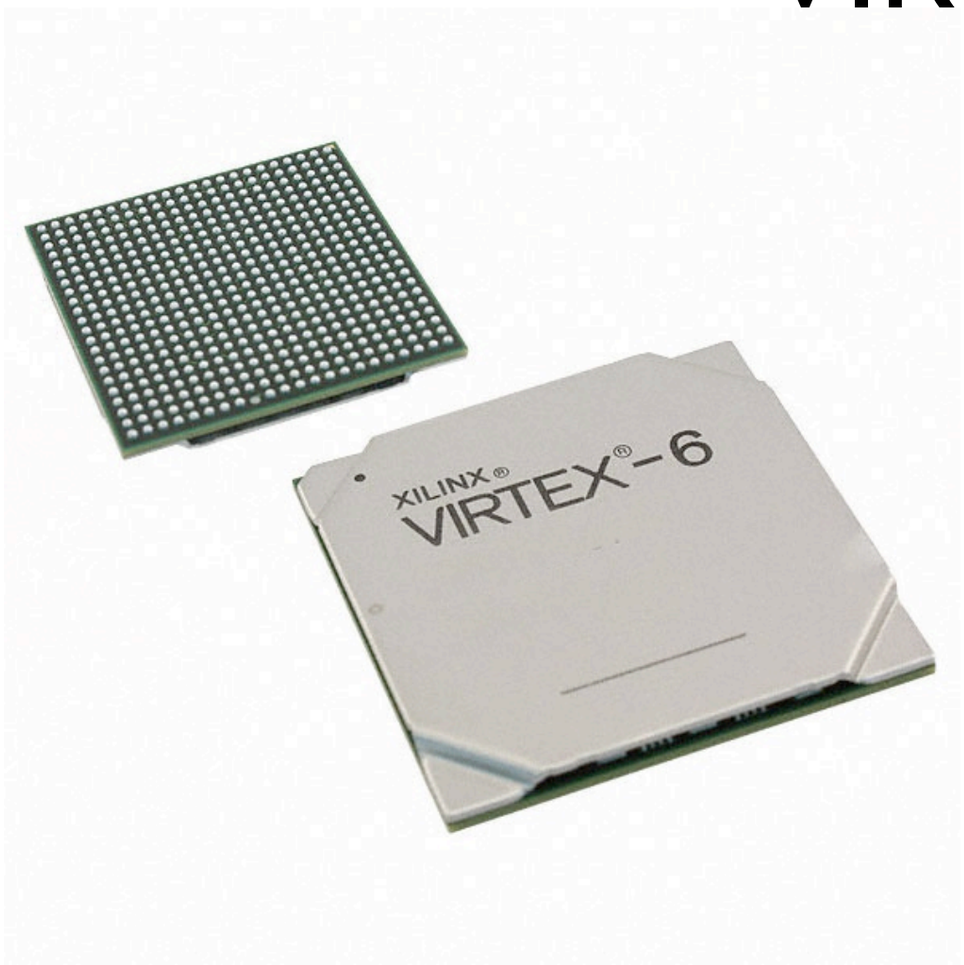

FlexRadio Systems
Software Defined Radios
HF/50MHz
Transceiver
FLEX-6700
Signature Series
MIC
PHONES
KEY
FlexRadio Systems
OK

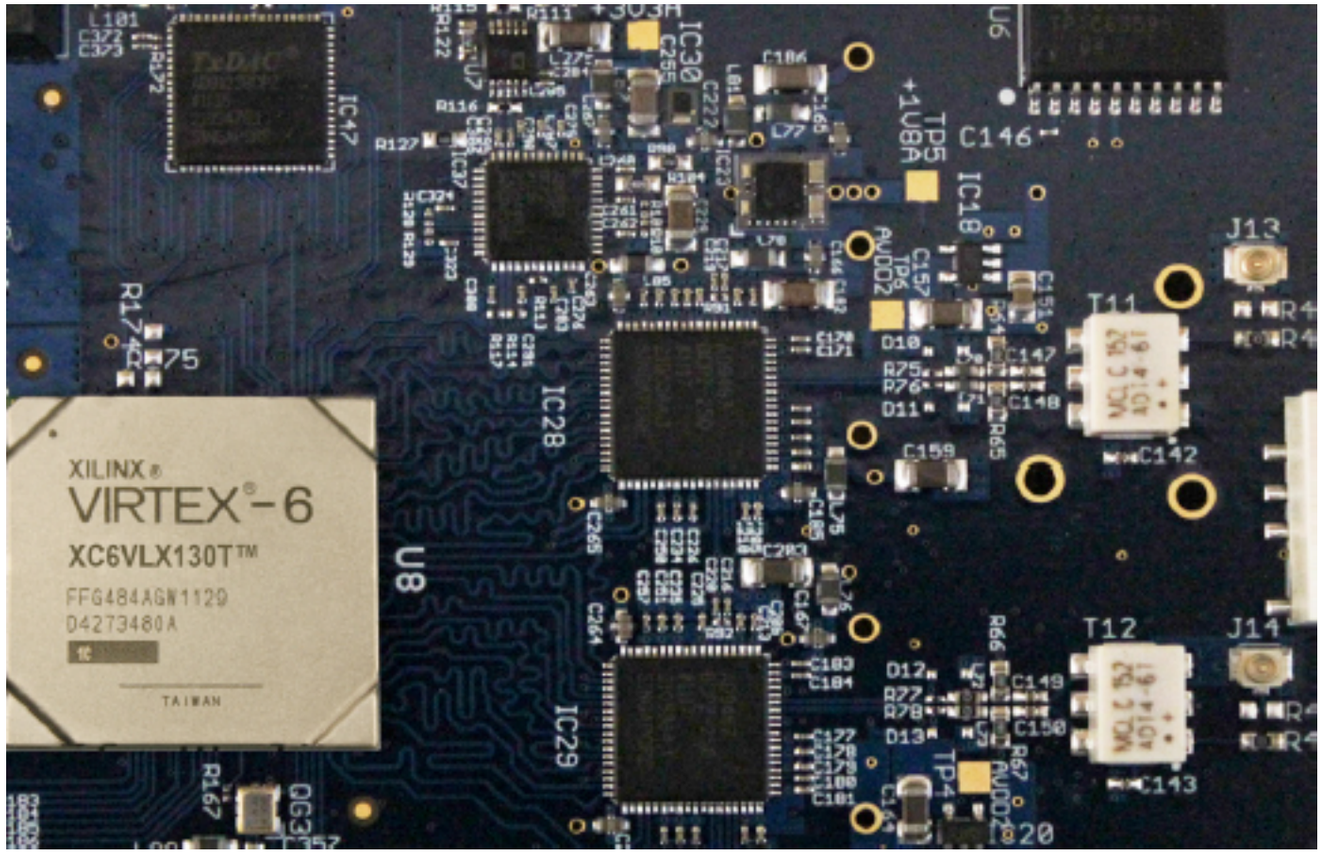
FLEX 6000



- SCU is a Spectral Capture Unit; 1 antenna per SCU
- Analog to Digital Converters sample at 245.76 Msps
- Uses a Xylinx Virtex-6 FPGA (XC6VLX130T)
- Allows 8 independent "Slice Receivers" from
  - 30kHz to 77MHz and 135MHz to 165MHz

VIRTEX-6 FPGA



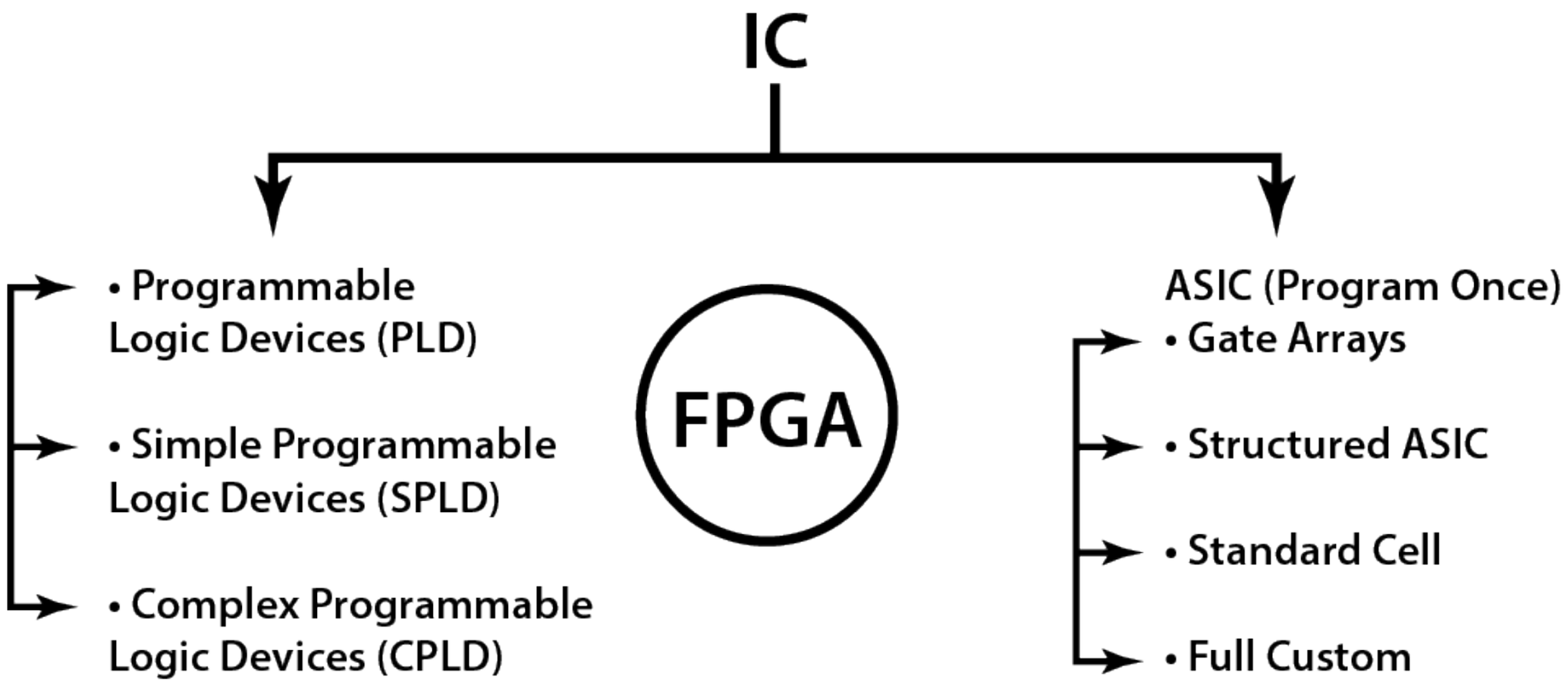


- Number of Logic Blocks (CLBs) - 20,000
- Number of Logic Elements - 128,000
- Number of I/Os - 240
- Package - 484 pin Flip-Chip Ball Grid Array (22x22)
- Price - $767.50

So What is an FPGA?

- FPGA means Field Programmable Gate Array
- It's a large Integrated Circuit that performs digital logic functions
- It's configurable (e.g. Programmable)
  - Logic Blocks (Programmable Logic Devices)
  - Input/Output (I/O) circuits or ports
  - Interconnects
- It also contains other circuits such as:
  - Random Access Memory (RAM)
  - Clock Manager
  - Dedicated Multipliers, Adders, and Counters
  - Ethernet ports
- The "logical units" in an FPGA are repeated in a matrix format - e.g. in rows and columns

SPECTRUM OF DIGITAL ICs



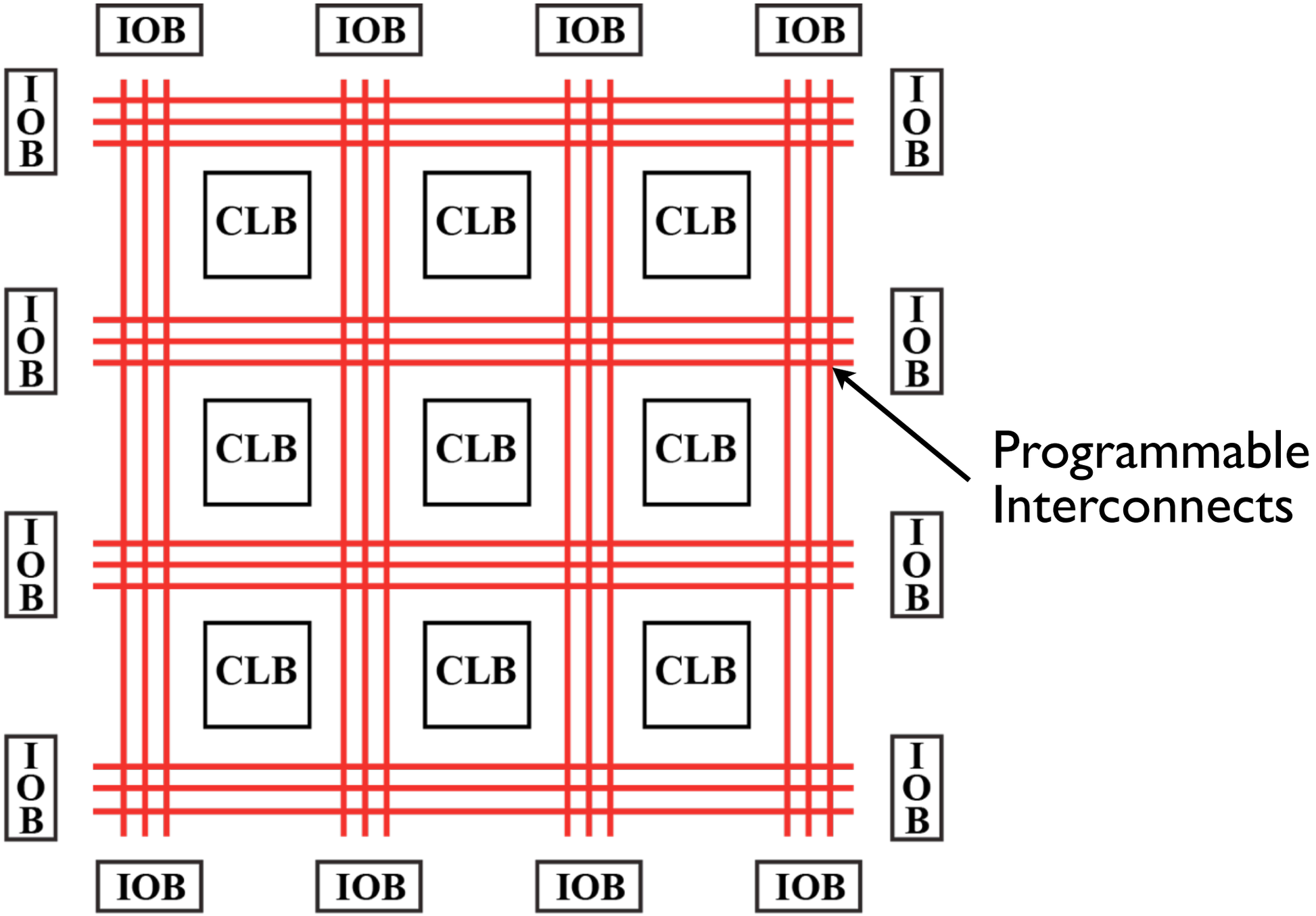
- Highly Configurable
- Fast Design Time
- Can't Support Complex Logic

- No Reconfiguration
- Time-Consuming Design
- Expensive
- Support Complex Functions

Applications For FPGAs

- Useful when the volumes do not support ASICS
- Digital Signal Processing
- Medical Imaging, CT Scanners, MRI, X-Ray
- Speech Recognition
- Cryptography
- Radio Astronomy
- Avionics
- Computer Networks and Routing
- Industrial Motor Control
- Some FPGAs now embedding ARM micro-processors.

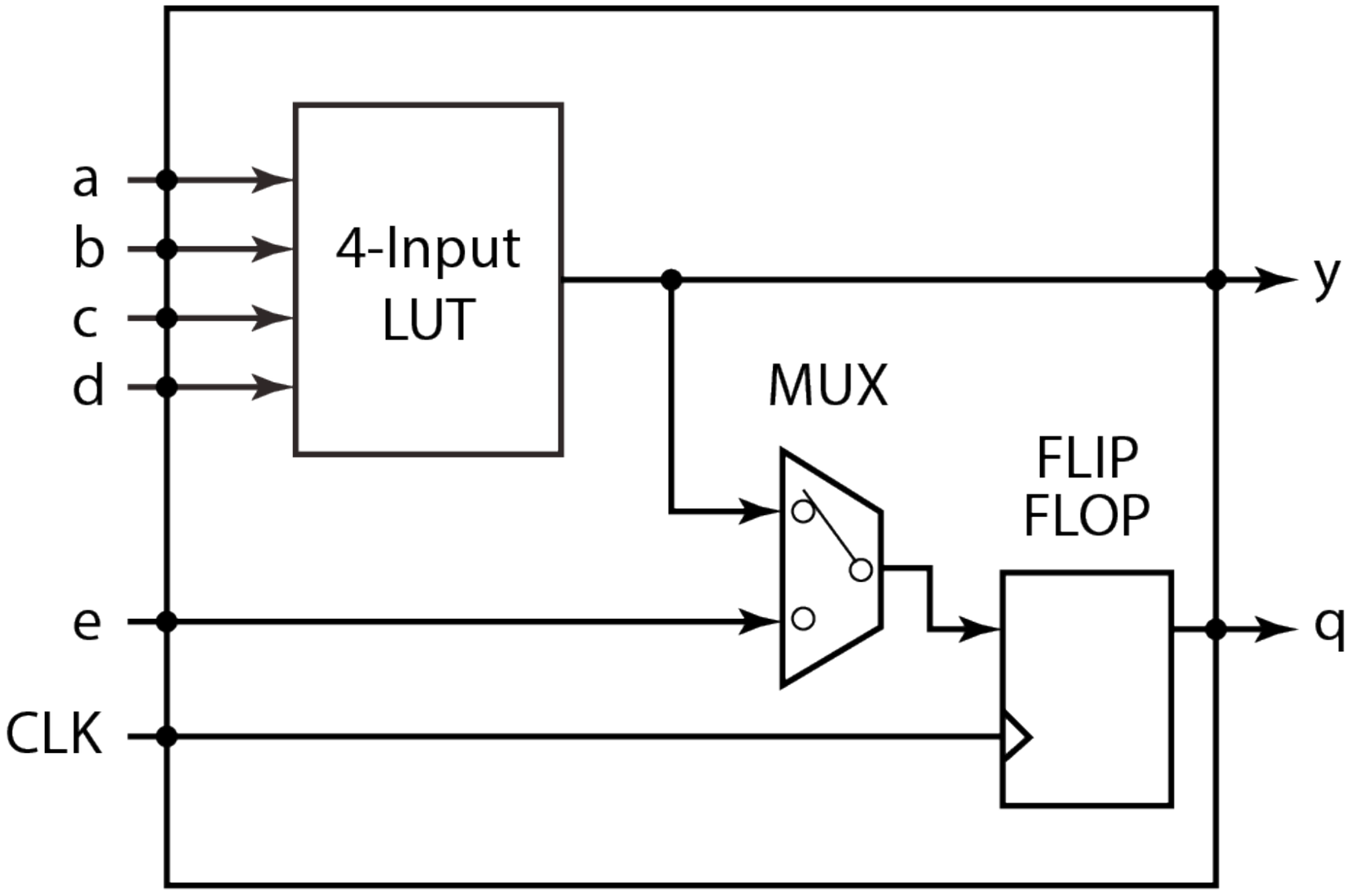
BASIC ORGANIZATION OF AN FPGA



CLB = CONFIGURABLE LOGIC BLOCK

IOB = INPUT/OUTPUT BLOCK

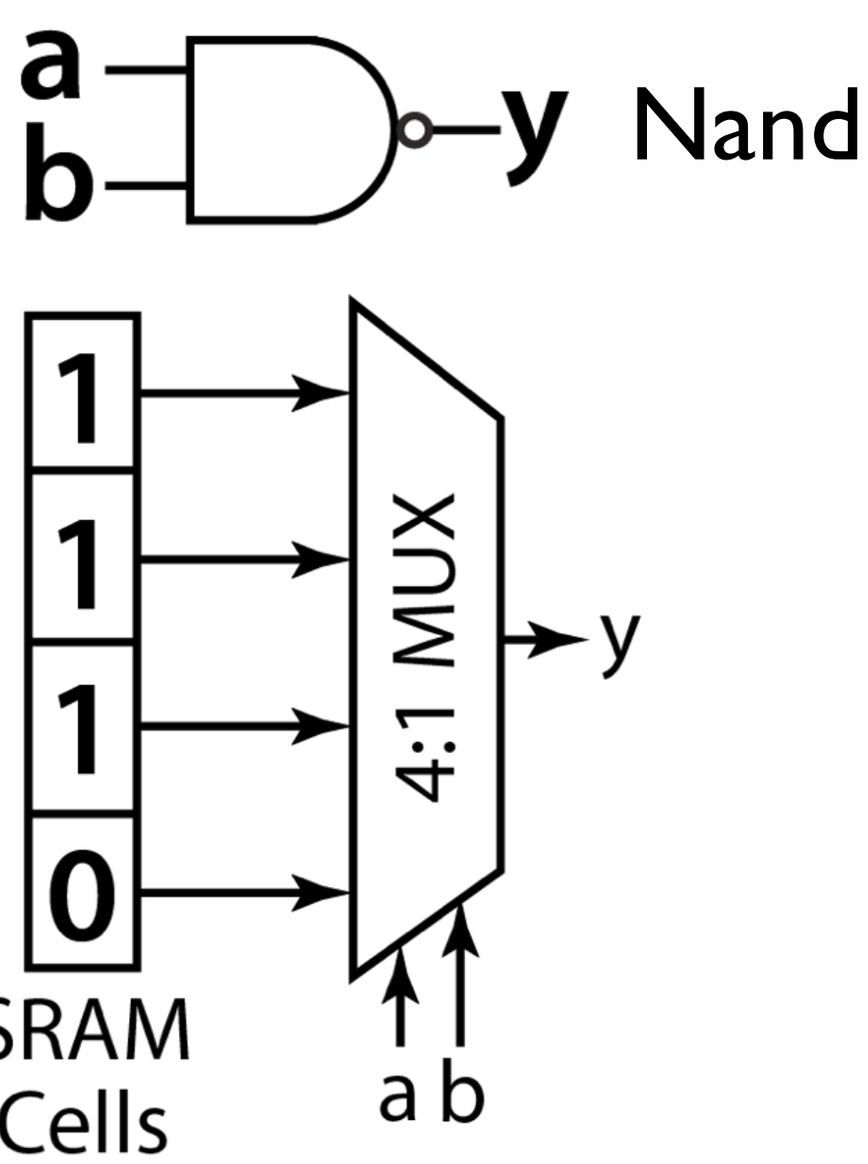
BASIC CONFIGURABLE LOGIC BLOCK (CLB)



- **LUT is a "Look Up Table" (more on next slide)**
- **MUX is a "multiplexer" or a switch**
- **The Flip Flop is a simple storage element**

WHAT IS A LOOK UP TABLE (LUT)?

Inputs		Output
a	b	y
0	0	1
0	1	1
1	0	1
1	1	0



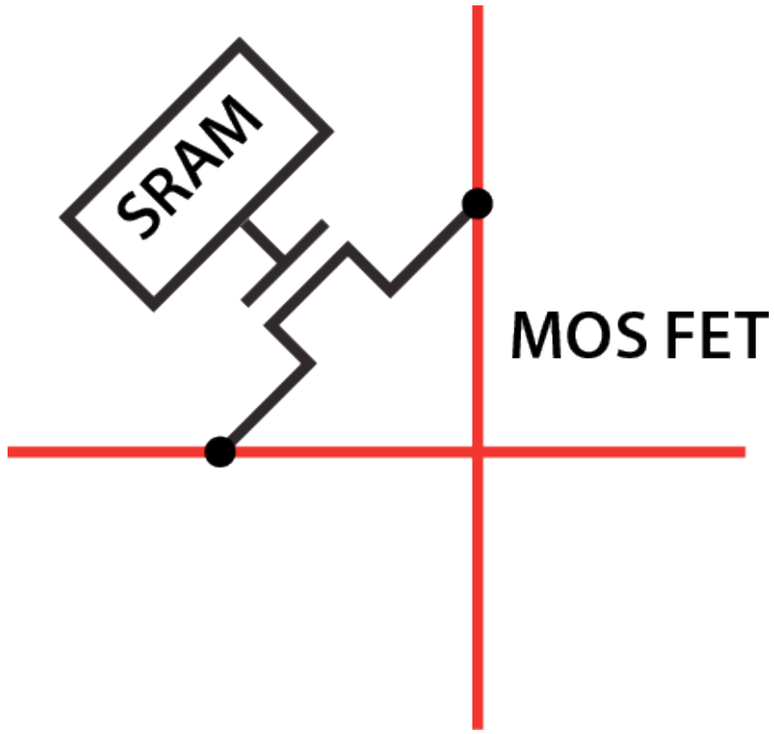
- The ALTERA EP3C40Q240C8N has a 4-input LUT
- The XYLINX XC6VLX130T has a 6-input LUT

Programming Methods

- Static RAM (SRAM) - based
  - Xilinx, Altera
  - Can reprogram
  - Data need to be read at "start-up"
- "Antifuse" technology
  - Actel, Quicklogic
  - "One-Time" programming
- EPROM/EEPROM - Not used very much

SRAM Method

- Can program SRAM to 0 or 1
- 0 disconnects lines; 1 connects line



- Can "Make" or "Break" cross-point connections
- Can define function of Logic Blocks
- SRAM cells are organized as a large "shift register" and programmed through "configurable pins" on the FPGA integrated circuit by a serial string of bits

WHY USE AN FPGA INSTEAD OF MICROPROCESSOR?

- FPGAs are faster - Why?
- Groups of CLBs in an FPGA can be combined to accomplish specific functions.
- Other CLB groups are combined to accomplish other functions
- All these different functions can be done simultaneously
- But a microprocessor must accomplish its tasks sequentially which takes longer

HOW ARE FPGAS PROGRAMMED?

- Similar to programming microprocessors
  - Integrated Development Environment (IDE)
  - Graphical User Interface (GUI)
  - Programming language (like Basic or C++)
  - Other software for converting the programming language into simple instructions the microprocessor can understand
- FPGA manufacturers provide software
  - Integrated Software Environment (ISE)
  - Graphical User Interface (GUI)
  - Programming language: Verilog or VHDL
  - Other software for
    - + Partitioning, Mapping, and Routing on the IC
    - + Simulating the design

WHAT DOES VERILOG CODE LOOK LIKE?

```
//------------------------------------------------------
// Design Name : up_counter
// File Name   : up_counter.v
// Function    : Up counter
// Coder       : Deepak
//------------------------------------------------------
module up_counter    (
out     ,  // Output of the counter
enable  ,  // enable for counter
clk     ,  // clock Input
reset      // reset Input
);
//----------Output Ports--------------
    output [7:0] out;
//------------Input Ports--------------
     input enable, clk, reset;
//------------Internal Variables--------
    reg [7:0] out;
//-------------Code Starts Here-------
always @(posedge clk)
if (reset) begin
  out <= 8'b0 ;
end else if (enable) begin
  out <= out + 1;
end


endmodule
```